Agenda

- Patent Policy:
  - The meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- Chip-Module Draft Baseline
- Chip-Chip Discussion and Draft Baseline
- Path forward

Minutes

- Attendees: Daniel Dove, **Pete Anslow**, Brian Misek, Derek Cassidy, Rick Rabinovich, David Brown, Alexander Umnov, Matt Brown, Galen Fromm, Kevin Burt, Tim Warland, Nathan Tracy, John Petrilla, Scott Irwin, Greg Lecheminant, Phil McClay, Stephen Docking, Ali Ghiasi, Mike Dudek, Tom Palkart, Mike Li
- Chip to Module
  - Discussion around BER used for jitter spec
    - For entire link to work at better than 1E-12, CAUI-4 specs should allow for better performance
    - If specs are too tight, high density applications (stacked connector) may have problems meeting requirements)
  - Discussion around peak amplitude requirement around 900mVpp
    - Will this cause an issue if we have high density passive cable as well as optical modules in a single system?
    - Note, CR4 allows for up to 1200mVppd,
    - Is this an implementation restriction since 900mVppd is a max
  - Change Stress Receiver tests to compare with VSR
- Chip to chip
  - Additional material required on required channel
  - Expected economies to be realized relative to 100GBASE-KR4
  - Call for material from System Vendors on what they would like to see in a chip-chip interface

Path Forward: CAUI-4 Consensus Presentation in San Antonio

- Make required modifications to latchman_01_11v2 and review Nov 7, 10am
- Additional presentation material needed on TBDs and other topics which the CAUI ad hoc has discussed
  - Chip-chip application targets, relative power to 100GBASE-KR4, implementation capabilities etc.
  - Eg. asymmetric link budget